PATENT APPLICATION

042390.P12396

Amendment

Amendment to Specification

Please amend the specification as shown below.

The paragraph on Page 2, line 5:

As the features and functionality of communication or computing systems increase [increases] it is often desirable to design such systems with more that one processor. Multi-processor systems may be desirable because then the processors may be tailored to specialize in particular tasks. For example, a digital signal processor that performs mathematically intense computations may be combined with an application processor that may be used to execute user applications.

A1

The paragraph on Page 5, line 11:

Portable communication device 50 may also comprise a memory device 30 that may include a memory array 35. Although the scope of the present invention is not limited in this respect, memory device 30 may be used to store data and or instructions to be executed by processors 70 and 80. Memory device 30 may comprise one or more memory types including, but not limited to, any type of disk storage including floppy disks, optical disks, CD-ROMs, magnetic-optical disks, read-only memories (ROMs), random access memories (e.g. static random access memories (SRAM), dynamic random access memories (DRAM), etc.), electrically programmable read-only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs), magnetic or optical cards, flash memory, or any other type of media suitable for storing electronic instructions and or data.

A2

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The paragraph on Page 6, line 19:

Although the scope of the present invention is not limited in this respect, portions 31-33 of memory device 30 may be adjacent or contiguous portion of memory array 35. In such an embodiment, portions 31-33 may share many of the signal or power supply lines used in the operation of memory device 30. For example, portions 31-33 may share the same [came] clock signals, reset signals, sense amps, power supply voltage potential lines, etc.

A3

The paragraph on Page 10, line 13:

Memory controller 210 may contain logic and/or decode circuitry to determine if processors 70 and 80 are permitted to access various portions of memory device 230. Memory controller, may also comprise collision detection circuitry to resolve conflicts should processors 70 and 80 simultaneously attempt to access the same portion of memory device 230. The use of a memory controller 210 should be considered optional [option], but may be desirable to reduce the sophistication or cost associated with memory device 230. By moving the arbitration and conflict logic from memory device 230 to a separate component (i.e. memory controller 210) there may be greater flexibility in the type of memory that may be used for memory device 230.

A4

Amendment to Title

Please change the title of the specification to:

MEMORY ADAPTED [ADAPTEDT] TO PROVIDE DEDICATED AND OR SHARED MEMORY TO MULTIPLE PROCESSORS AND METHOD THEREFOR